

**What is claimed is:**

1        1.    A method of reducing step height, comprising:  
2        providing a substrate comprising a low-voltage device  
3                area and high-voltage device area divided by an  
4                isolation structure and a pad oxide layer on the  
5                surface of the low-voltage device area and high-  
6                voltage device area;  
7        sequentially forming a silicon nitride layer of at  
8                least about 500Å thick and a patterned mask  
9                layer, exposing the silicon nitride layer on the  
10               high-voltage device area and parts of the  
11               isolation structure adjacent thereto, overlying  
12               the substrate;  
13        anisotropically etching the exposed silicon nitride  
14               layer using the mask layer as an etch mask,  
15               exposing the high-voltage device area and parts  
16               of the isolation structure;  
17        sequentially removing the patterned mask layer and pad  
18               oxide from the surface of the high-voltage device  
19               area;  
20        forming a first oxide layer on the exposed high-voltage  
21               device area and isolation structure using the  
22               silicon nitride layer as a mask;  
23        sequentially removing the remaining silicon nitride  
24               layer and pad oxide layer from the surface of the  
25               low-voltage device area; and  
26        forming a second oxide layer, thinner than the first  
27               oxide layer, on the low-voltage device layer.

1        2.    The method as claimed in claim 1, wherein the  
2    isolation structure comprises a shallow trench isolation  
3    (STI) structure or field oxide (FOX) layer.

1        3.    The method as claimed in claim 1, wherein the  
2    first oxide is formed by thermal oxidation.

1        4.    The method as claimed in claim 1, wherein the  
2    first oxide layer thickens gradually to a predetermined  
3    value and approximately maintains the thickness in areas  
4    further from the low-voltage device structure.

1        5.    The method as claimed in claim 1, wherein the  
2    first oxide layer is about 1000 to 2000Å thick.

1        6.    The method as claimed in claim 1, wherein the  
2    second oxide layer is formed by thermal oxidation.

1        7.    The method as claimed in claim 1, wherein the  
2    second oxide layer is about 32 to 125Å thick.

1        8.    The method as claimed in claim 1, wherein the  
2    silicon nitride layer on the low-voltage device area is  
3    removed by hot phosphoric acid.

1        9.    A method of reducing step height, comprising:  
2        providing a substrate having a low-voltage device area  
3                and high-voltage device area divided by an  
4                isolation structure;  
5        forming an oxidation mask at least approximately 500Å  
6                thick over the low-voltage device area and parts  
7                of the isolation structure;

8 forming a first oxide layer on the exposed high-voltage  
9 device area and isolation structure using the  
10 oxidation mask as a mask;  
11 removing the oxidation mask; and  
12 forming a second oxide layer, thinner than the first  
13 oxide layer, on the low-voltage device layer.

1 10. The method as claimed in claim 9, wherein the  
2 isolation structure comprises a shallow trench isolation  
3 (STI) structure or field oxide (FOX) layer.

1 11. The method as claimed in claim 9, wherein the  
2 oxidation mask is a silicon nitride layer.

1 12. The method as claimed in claim 9, wherein the  
2 first oxidation layer is formed by thermal oxidation.

1 13. The method as claimed in claim 9, wherein the  
2 first oxide layer thickens gradually to a predetermined  
3 value and approximately maintains the thickness in areas  
4 further from the low-voltage device structure.

1 14. The method as claimed in claim 9, wherein the  
2 first oxide layer is about 1000 to 2000Å thick.

1 15. The method as claimed in claim 9, wherein the  
2 second oxidation layer is formed by thermal oxidation.

1 16. The method as claimed in claim 9, wherein the  
2 second oxide layer is about 32 to 125Å thick.

1 17. The method as claimed claim 9, wherein the  
2 oxidation mask is removed by hot phosphoric acid.

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1        18. The method as claimed in claim 9, further  
2 comprising a pad oxide layer on the surface of the low-  
3 voltage device area and high-voltage device layer.

1        19. The composite as claimed in claim 9, further  
2 comprising removing the pad oxide layer from the low-voltage  
3 device layer when the oxidation mask is removed.